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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,971	06/25/2003	Benjamin Brown	1563-US	6459

7590 11/02/2004

Legal Department
Teradyne, Inc.
321 Harrison Avenue
Boston, MA 02118

EXAMINER	
SUAREZ, FELIX E	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,971	BROWN ET AL.	
	Examiner	Art Unit	
	Felix E Suarez	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Minor Informalities

1. The disclosure is objected to because of the following informalities:

In page 5 line 35 of the specification, blank space "_____," should be completed.

In Claim 15 page 17, line 12 the phrase "paket" should be --packet --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 4, 5, 8, 10, 11, 14 and 15-18 are rejected under 35 U.S.C. 102(e) as being unpatentable over Volkerink et al. (U.S. Patent Application Publication No. 2004/0107395).

With respect to claims 1, 8 and 14, Volkerink et al. (hereafter Volkerink) teaches an automatic test equipment (or method) for testing, non-deterministic packet data from a device-under-test, the automatic test equipment including:

a memory for storing (see page 5 paragraph [0040]) expected packet data (see page 9 paragraph [0066]);

a receiver for receiving the packet data from the device-under-test (see page 5, paragraphs [0038]-[0040]); and

a data validation circuit coupled to the receiver for validating the non-deterministic packet data based on the expected packet data from the memory (see page 5, paragraphs [0038]-[0040], [0043]).

With respect to claims 4 and 10, Volkerink further teaches that the memory expected packet data includes predetermined signatures representing valid packet data combinations from the device-under-test, the non-deterministic packet data validation circuit including:

a signature generator for creating actual signatures based upon actual data combinations received from, the receiver (see page 5 paragraph [0041]); and

a comparator for comparing the actual signatures to the predetermined signatures to identify valid packet data (see page 5, paragraphs [0041], [0043]).

With respect to claims 5 and 11, Volkerink further teaches including:

a capture memory coupled to the receiver for storing the packet data received by the receiver (see page 6, paragraphs [0048]-[0049] and page 7 paragraph [0055])).

With respect to claim 15, Volkerink further teaches that the validating step includes:

pipelining the received data such that the first packet received is the first packet validated (see page 5, paragraphs [0038]-[0040]);

comparing, in the order received, each actual packet to the stored, expected packet data in the memory (see page 6 paragraph [0048]); and

validating the non-deterministic packet data based on the comparing step (see page 5, paragraphs [0038]-[0040], [0043]).

With respect to claims 16, Volkerink further teaches that the expected data includes idle data, the method further includes the step:

filtering the idle data to generate filtered expected data, and wherein the comparing step includes comparing, in the order received, each actual packet to the filtered expected data (see page 11 paragraph [0080]).

With respect to claim 17, Volkerink further teaches that the memory stores predetermined valid signatures representing valid packet data combinations from the device-under-test, and wherein the validating step includes:

generating an actual signature for each received data packet (see page 5 paragraph [0041]);

comparing the generated actual signature to the predetermined valid signatures (see page 5, paragraphs [0041], [0043]); and

determining whether the received data packet passed or failed based on the comparison of the signatures (see page 7 paragraph [0053] and pages 7-8, paragraph [0058]).

With respect to claim 18, Volkerink further teaches that the step of generating an actual signature includes:

calculating a checksum from the received packet data (see page 8 paragraph [0061] and page 12, paragraphs [0088], [0091]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2, 3, 6, 7, 9, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Volkerink et al. (U.S. Patent Application Publication No. 2004/0107395) in view of DeSouza et al. (U.S. Patent No. 5,245,617).

With respect to claims 2 and 9, Volkerink teaches all the features of the claim invention, except that Volkerink does not teach:

a first-in-first-out circuit having an input coupled to the receiver and an output; nor

a comparator having a first input coupled to the first-in-first-out circuit and a second input coupled to the memory, the comparator operative to compare the. first-in-first-out output to the expected packet data from the memory.

But DeSouza et al. (hereafter DeSouza) teaches in a First-In-First-Out (FIFO) memory circuit that, its primary elements, a deserializer, a cyclic redundancy check (CRC) checker and a receiver state machine, interconnect with the encoder/decoder, receiver FIFO and system interface. As described above, the deserializer accepts the incoming serial NRZ (non-return-to-zero) data and recovered received data clock from the encoder/decoder and converts it to eight-bit wide bytes of data for transfer to the receiver FIFO. The CRC checker calculates the four-byte frame check sequence (FCS) field from the incoming data stream and compares it with the last four bytes of the received packet of

data to verify data integrity. The receiver state machine further generates control signals for instructing the receiver FIFO to store its incoming data and processes CRC error signals received from the CRC checker (see DeSouza; col. 2, lines 26-46).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Volkerink to include the FIFO memory circuit as taught by DeSouza, because the FIFO memory circuit of DeSouza allows to compares the incomes data stream with the last four bytes of the received packet of data to verify data integrity.

With respect to claim 3, Volkerink in combination with DeSouza teaches all the features of the claimed invention, and Volkerink further teaches including:

a filter having an input coupled to the memory and an output coupled to the comparator second input, the filter configured to mask idle packet data (see Volkerink; page 11 paragraph [0080]).

With respect to claims 6 and 12, Volkerink in combination with DeSouza teaches all the features of the claimed invention, and DeSouza further teaches that the signature generator comprises a CRC arithmetic register (see DeSouza; col. 2, lines 26-46).

With respect to claims 7 and 13, Volkerink in combination with DeSouza teaches all the features of the claimed invention, and Volkerink further teaches that the CRC arithmetic register comprises a linear feedback shift register (see Volkerink; page 2 paragraph [0011]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Volkerink et al. (U.S. Patent Application Publication No. 2004/0107395) in view of Chirashnya et al. (U.S. Patent No. 6,601,195).

With respect to claim 19, Volkerink teaches a method for validating non-deterministic packet data from a device-under-test using automatic test equipment, the automatic test equipment having a memory, the method including the steps:

testing the device-under-test (see page 7 paragraph [0055]);

generating a signature of actual data captured during the testing step (see page 7 paragraph [0053]);

generating a new signature for the evaluated captured data (see page 7 paragraph [0056]).

Volkerink does not teach:

establishing a library of known passing/failing signatures in the memory;

comparing the generated signature from the captured data to the library of known passing/failing signatures;

determining a pass/fail result for the device test if the compared signature matches a signature in the library;

evaluating the captured data to determine whether the device passed/failed if the compared signature does not match the library; nor

adding the new signature to the library of known passing/failing signatures.

But Chirashnya et al. (hereafter Chirashnya) teaches in a switch adapter testing that, when the user invokes a test on the control workstation (CWS), a Test Invocation Module (TIM) creates a Test Definition File (TDF), initializes a POWERParallel diagnostics system (SPD) Message Daemon Server and invokes a SPD graphical user interface (GUI) program. After this whole environment was created on the CWS, the TIM remotely invokes an i_stub program on the primary node. This program generates a diagnostics request to the system management module, called a fault-service daemon (FSD). The FSD

is an event-driven program that idles most of the time waiting for received events, such as error packets from any network component. When FSD receives a diagnostics request, it changes its run mode to the diagnostics mode. In this mode, all received events are first handled by the diagnostics models, and only after that might be forwarded to the FSD for further processing. First, FSD loads a dynamically-loadable library SPDLib. When SPDLib is loaded, FSD resolves all hook functions for diagnostic processing. There are several such functions that are called only when diagnostics are running (see Chirashnya; col. 24, lines 32-50).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Volkerink to include the fault-service daemon (FSD) as taught by Chirashnya, because the FSD of Chirashnya allows to load a dynamically-loadable library SPDLib and when SPDLib is loaded, FSD resolves all hook functions for diagnostic processing; as desired for comparing signatures (see Volkerink; page 6 paragraph [0048]), for determining a pass/fail result (see Volkerink; page 7 paragraph [0053]), for evaluating the captured data (see Volkerink; page 7 paragraph .

comparing the generated signature from the captured data (see Volkerink; page 6 paragraph [0048]);

determining a pass/fail result for the device test (see Volkerink; page 7 paragraph [0053]);

evaluating the captured data to determine whether the device passed/failed (see Volkerink; page 7 paragraph [0053]); or

adding the new signature (see page 8 paragraph [0061] and page 12, paragraphs [0088], [0091]).

Conclusion

Prior Art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hollander [U.S. Patent No. 6,530,054] describes an apparatus for testing a device under test.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Felix Suarez, whose telephone number is (571) 272-2223. The examiner can normally be reached on weekdays from 8:30 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on (571) 272-2216. The fax phone numbers for the organization where this application or proceeding is assigned is 703-872-9306 for regular communications and for After Final communications.

October 25, 2004

F.S.

PATRICK ASSOUAD
PRIMARY EXAMINER